DETAILED ACTION

Claim Objections

1. Claim 96 objected to because of the following informalities: Claim 96 is written as being dependent on claim 50 as well as claim 49. Claim 50 has been withdrawn from consideration. Appropriate correction is required.

2. Applicant is advised that should claims 108 and 114 be found allowable, claim 114 will be objected to under 37 CFR 1.75 as being a substantial duplicate of claim 108. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 49, 66, 81, 90, 91, 96, 103, 104, 105, 106, 108-110, 113 and 114 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al (US 6,110,823) in view of Guldenpfennig (US patent 3,878,145) and Shibayama et al (US patent 4,039,415).

6. As indicated in the previous office action, the Eldridge et al patent (hereinafter Eldridge) is directed to a method for forming contact structures. The contact structures are formed by bonding a free end of a wire to a substrate, and subsequently overcoating the wire with a least one layer of material. See the abstract. The contact structures of Eldridge may be used as probes (column 14, lines 25-32). Thus, Eldridge is directed to the same field of endeavor as applicant's invention which, as indicated in the title, is directed to methods of fabrication of probe structures.

7. Figures 5 of Eldridge illustrates a wire which has been coated with at least two layers of material to create a resilient contact structure (column 16, lines 15-18). Wire 502 has a first (proximal) end and a second (distal) end. The first end is bonded to terminal 512 (column 46, lines 55-63). This corresponds to the “providing” and “bonding” steps of claim 49. Figure 5 shows conductor 502 coated with inner coating layer 520 and outer coating layer 522. Eldridge teaches that the outermost (top) layer or both layers is/are a conductive material (column 47, lines 15-18; lines 38-39). This clearly indicates that the inner layer may be other than a conductive material, i.e., a dielectric material. Eldridge additionally teaches coating a dielectric layer onto a wire in the embodiment of figure 10k which includes a layer of dielectric material 1094 (column 67, lines 55-59). This corresponds to the "forming a dielectric coating" step of claim 49. Eldridge teaches that generally, the vertical end portions (as illustrated) of the wire

stem do not contribute to the overall resiliency of the contact structure. The coating need not cover the second end which may be exposed as shown in figure 5B (column 48, lines 16-29). This teaching corresponds to the limitation in applicant's claim 49 that there is an exposed portion of the elongated conductor at the second end that is not coated with the dielectric coating. As indicated in the abstract and column 1, lines 26-42, the method of Eldridge is for forming a plurality of connections.

8. Applicant has amended claim 49 to recites that the dielectric coating is formed electrochemically. The Guldenpfennig patent is directed to a process for electrochemically forming a coating based on epoxy resin esters (column 1, lines 22-34). Guldenpfennig discloses that the coating may be used for electro isolating (insulating) of wires (column 15, lines 44-45).

9. The Shibayama et al patent (hereinafter Shibayama) is directed to a process for electrochemically depositing insulation on a wire. See the abstract. As shown in example 2, an epoxy resin may be used to form the coating. An insulated wire having a coating with a thickness of 26μm and an excellent appearance was obtained.

10. The prior art of record is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious at the time the invention was made to have applied the dielectric coating of Eldridge electrochemically because Guldenpfennig and Shibayama teach that electrochemical deposition is capable of forming on a wire an insulating coating with desirable properties.

11. With respect to claim 66, as noted above, Guldenpfennig and Shibayama disclose electrochemically depositing insulating layers based on an epoxy.

12. With respect to claims 81, Eldridge et al shows in several figures, including figures 5, 5b and 10k, that the conductor has a shape which is partially curved and partially linear.

13. With respect to claim 90, Eldridge et al discloses that the resilient contact structures may be used as probes (column 14, lines 28-29). A resilient and/or compliant (springy) contact structure which is securely mounted to an electronic component may be used for effecting temporary connection of the electronic component to another electronic component (column 12, lines 43-47). The resilient contact structures can be used to temporarily connect an electronic component for procedures such as burn-in and testing of the electronic component (column 14, lines 44-47).

14. With respect to claim 91, Eldridge et al discloses that it is known to utilize a test device with a plurality of wires in high density PCB and IC (integrated circuit) testing applications (column 5, lines 1-11).

15. With respect to claim 96, figures 5 and 5b of Eldridge et al shows conductor 502 with first end 502a bonded to a terminal 512 on substrate 508. The second end is formed with ball (protuberance) 534. See column 46, lines 55-62. This ball is a protuberance as recited in claim 96.

16. With respect to claim 103, the figures of Eldridge indicate that the coating is conformal and substantially uniform. As noted above, Shibayama discloses that an insulated wire having a thickness of 26μm was obtained in example 2, suggesting a uniform coating.

17. Claims 104 and 106 recite that the exposed portion is at the second end and is formed by not coating the end. Eldridge shows in figure 5B an exposed portion at the second end. Since the end it to remain exposed, it would have been obvious not to have coated it.

18. Claims 105, 108-110, 113 and 114 recite that the dielectric coating does not contain a metal constituent. The epoxy based coatings of Guldenpfennig and Shibayama do not contain a metal constituent.

19. Claims 86, 88, 92, 93, 94, 107, 111 and 112 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al (US 6,110,823) in view of Guldenpfennig (US patent 3,878,145) and Shibayama et al (US patent 4,039,415) as applied to claims 49, 81, 90, 91, 96, 103, 104 and 106 above, and further in view of Nakata et al (US 5,665,610).

20. Eldridge et al recognizes that modern integrated circuits are generally produced by creating several, typically identical, integrated circuit dies on a single semiconductor wafer (column 73, lines 1-4). "Burn-in" is a process whereby a chip (die) is either simply powered up or is powered up and signals exercising some degree the functionality of the chip are applied. It is known to perform burn-in prior to singulating the dies. Typically, the temporary connections to the dies are made by test probes or by "flying wires". See column 73, lines 15-26.

21. Claim 86 differs from Eldridge et al by reciting that the plurality of conductors are distributed into a plurality of groups, while claim 88 recites that the groups are arranged in an array. Claim 92 recites the groups correspond to integrated circuit chips on a substrate and claim 93 recites a plurality of integrated circuit chips. The Nakata et al patent is directed to a semiconductor device checking method. Nakata et al teach that in order to guarantee the quality of bare (unpackaged) chips, it is necessary to perform checks such as burn-in while the device is part of the wafer. Nakata et al recognize that it takes a long time to check a plurality of bare chips formed on the wafer one by one. Consequently, it is required that a check such as burn-in

should be made on a plurality, for example, 1000 or more bare chips while the chips are part of the wafer. A supply voltage and a signal to the check electrodes of a plurality of semiconductor chips formed on the wafer are simultaneously applied so as to operate the chips. It is necessary to prepare a probe card having a large number of probe terminals. See column 1, lines 27-46. Figure 3 shows an example of a semiconductor wafer housing for causing bump15 of the contactor 14 to come in contact with the check electrode 11 of the semiconductor chip 10. See column 5, lines 41-44. As illustrated in figure 3(a) and 3(b), bumps 15 are distributed in a plurality of groups of four which form an array. It would have been obvious at the time the invention was made to have formed the plurality of conductors in Eldridge into an array of groups as illustrated by Nakata et al because it would have facilitated testing each chip of a plurality of chips on a single wafer.

22. Claim 94 recites holding the substrate for retractably moving the substrate toward an electronic device and applying electrical signals to the conductors. Nakata et al disclose that in figures 3(a) and 3(b) element 21 is a holding plate for holding semiconductor wafer A. As shown in the figures, contactor 14 is adapted to be brought into contact with wafer A. See column 5, lines 45-54. As noted above, signals are supplied to the check electrodes so as to operate the chips. It would have been obvious at the time the invention was made to have provided a housing for retractably moving the substrate toward the conductors of Eldridge in a testing procedure as taught by Nakata et al because temporary contact with the wafer being tested would have been obtained.

23. Claim 107 recites that the exposed portion is at the second end and is formed by not coating the end. This is the same limitation recited in claims 104 and 106 and discussed above.

Eldridge shows in figure 5B an exposed portion at the second end. Since the end it to remain exposed, it would have been obvious not to have coated it.

24. Claims 111 and 112 recite that the dielectric coating does not contain a metal constituent. The epoxy based coatings of Guldenpfennig and Shibayama do not contain a metal constituent.

Response to Arguments

25. Applicant's arguments with respect to claims 49, 66, 81, 86, 88, 90-94, 96 and 103-114 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM LEADER whose telephone number is (571)272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexa D. Neckel can be reached on 571-272-1446. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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